

Tune Tracker at Fermilab: Status

C.Y. Tan
26/27 Feb '04

Overview

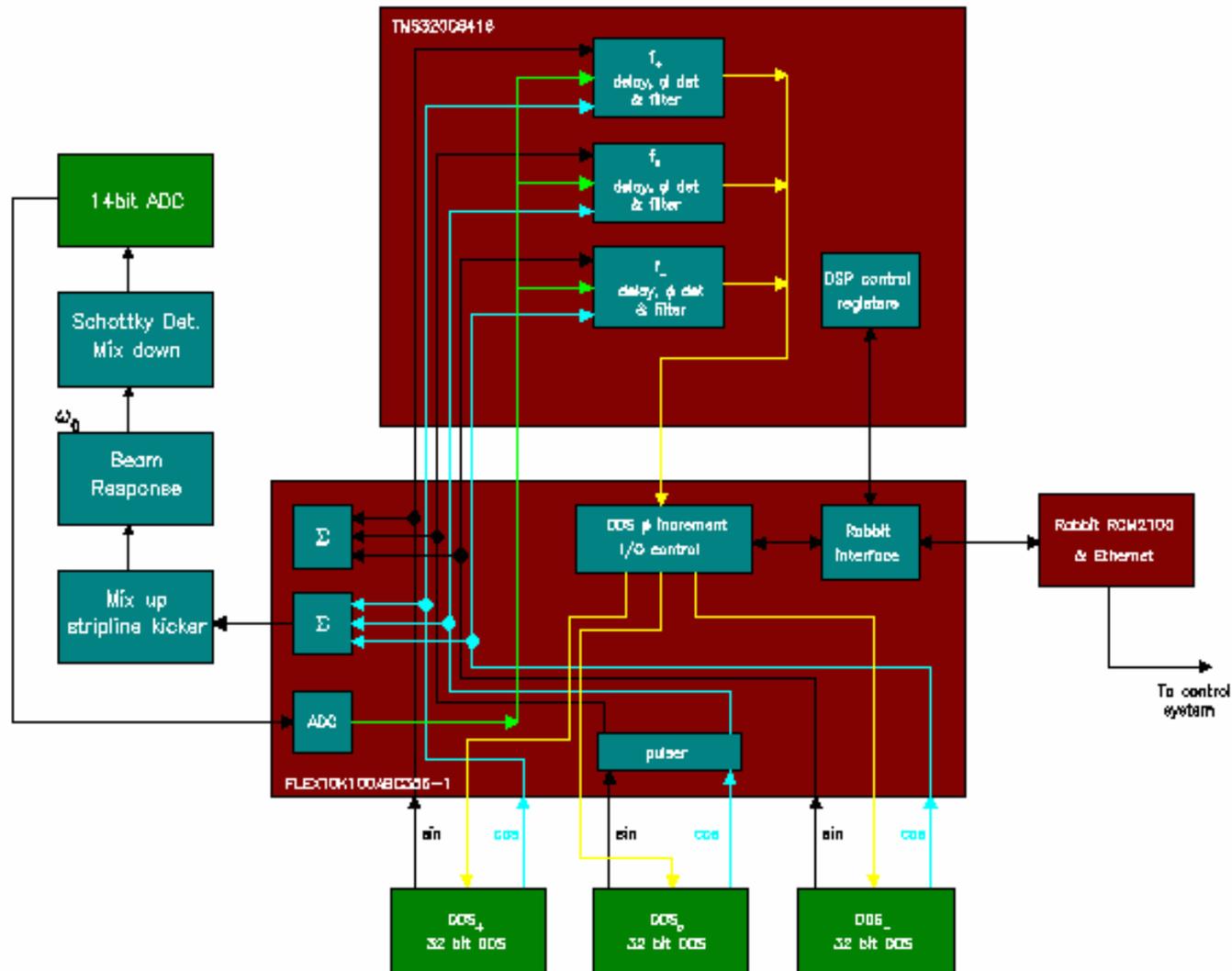
- PLL hardware status
 - ▶ Hardware consists:
 - DSP board
 - ADC, DAC, DDS daughter board
 - Schottky detector, kicker and RF modules
- PLL software status
 - ▶ DSP software
 - ▶ ALTERA firmware
 - ▶ Rabbit microcontroller software
 - ▶ Control system software

People Involved as of 26/27 Jan 04

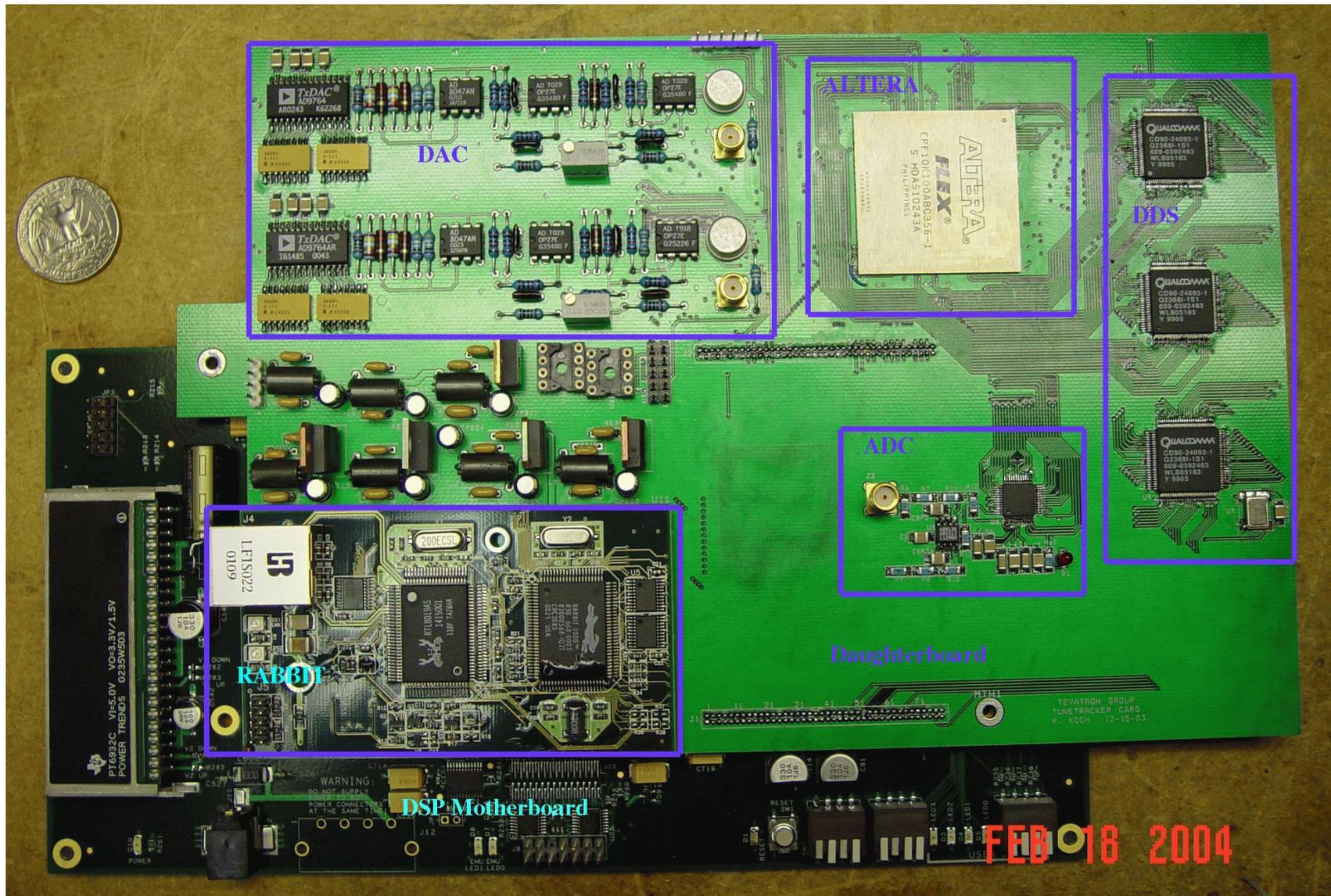
- Cheng-Yang Tan
 - ▶ Design
 - ▶ Simulations
 - ▶ Calculations (A. Burov is working on this).
- Ken Koch
 - ▶ Orcad layout and fabrication
- Jia Ning
 - ▶ Working on electronic beam simulator
- Army of 1.5 to 1.7

Hardware

Hardware Block Diagram



Completed DSP and Daughterboard



Hardware Description

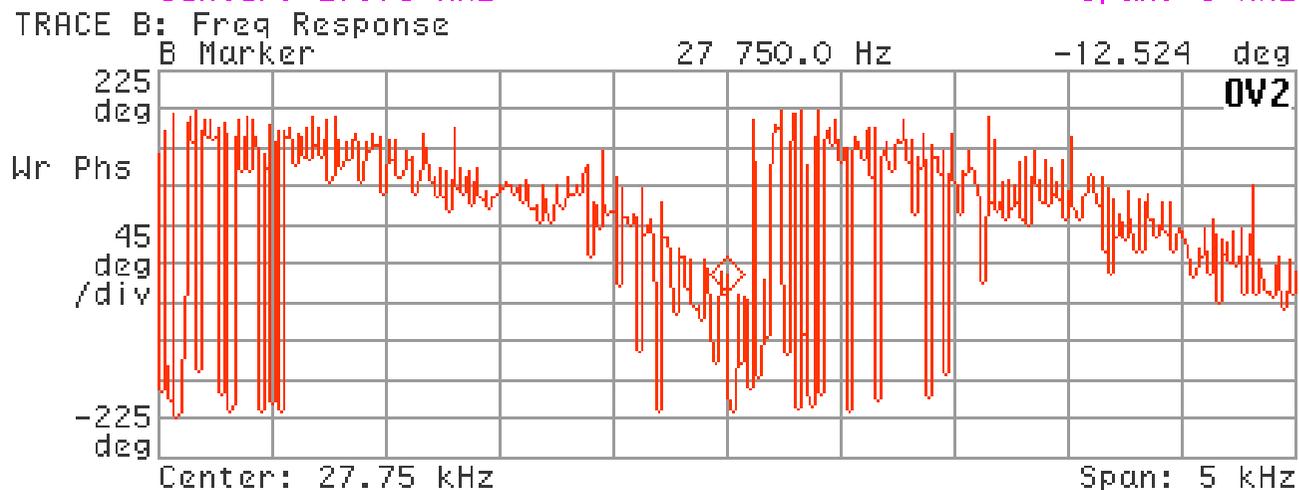
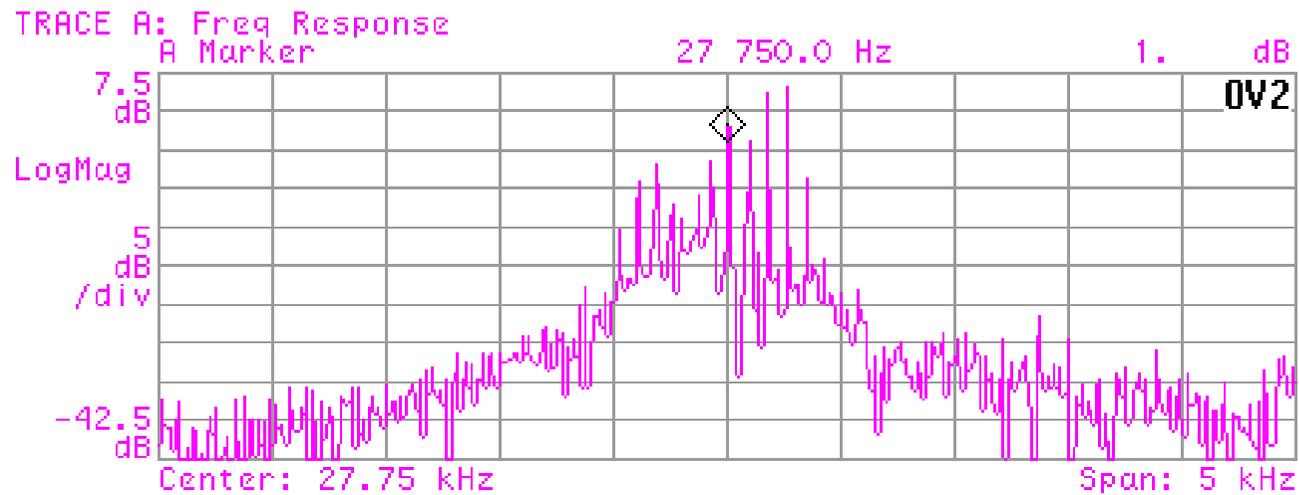
- Software PLL using TMS320C6416@500MHz
- THS14F03 14 bit ADC (3 MHz)
- AD9764 14 bit DAC
- 3 Q2368 32 bit DDS (clk freq 25MHz)
- ALTERA FLEX10K100ABC356 as interface between ADC, DAC, DDSs and DSP
- Rabbit RCM2100 microcontroller for communications with outside world.

Why 3 DDSs?

- General idea is to sandwich 2 DDS frequencies with 1 DDS which found the centre.
- Will be clearer as we move on ...

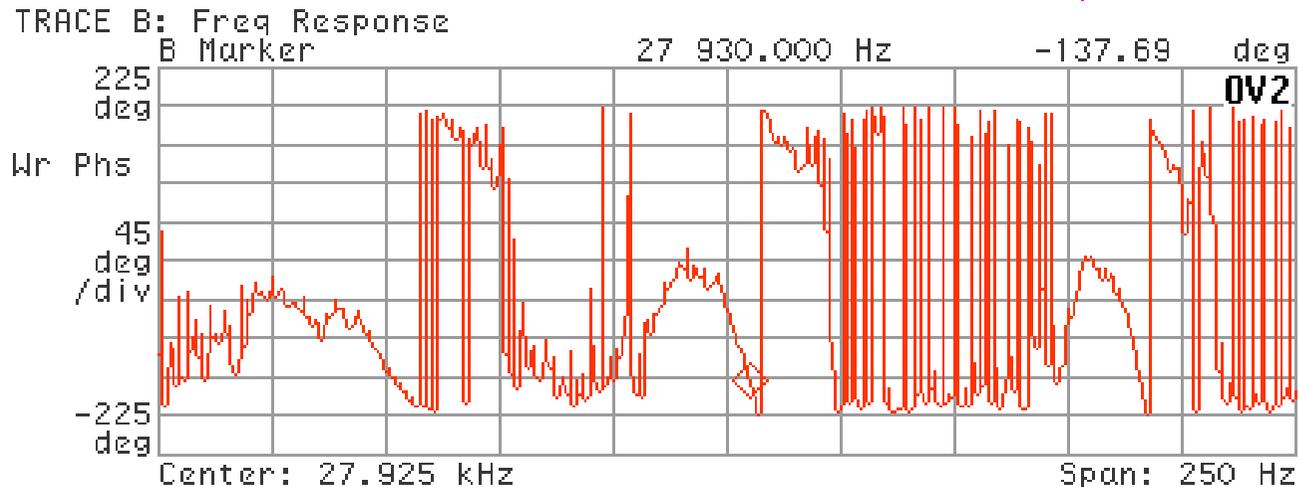
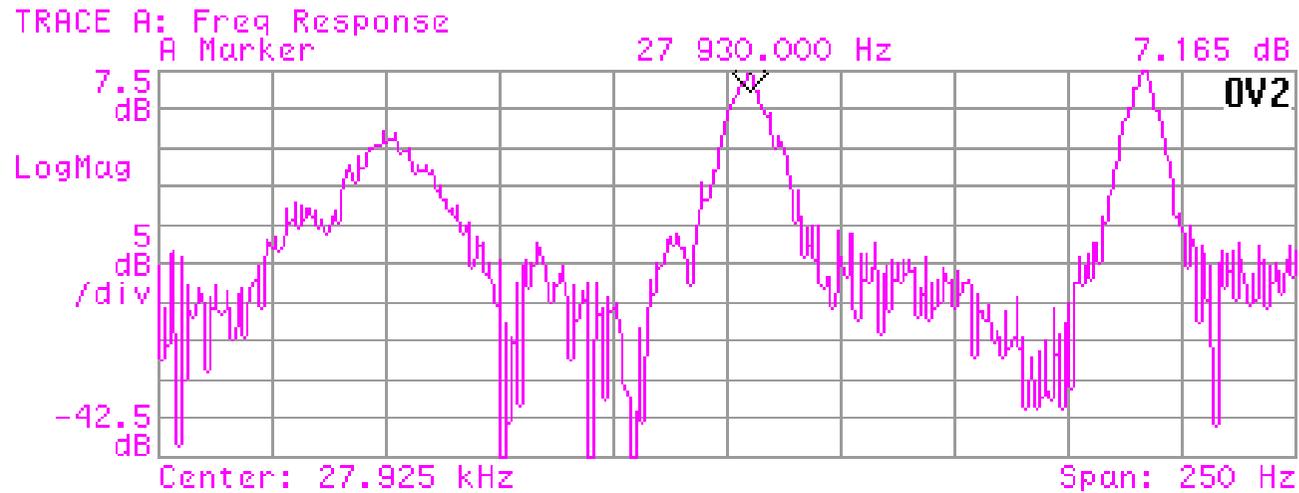
Frequency response

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Frequency Response of Beam

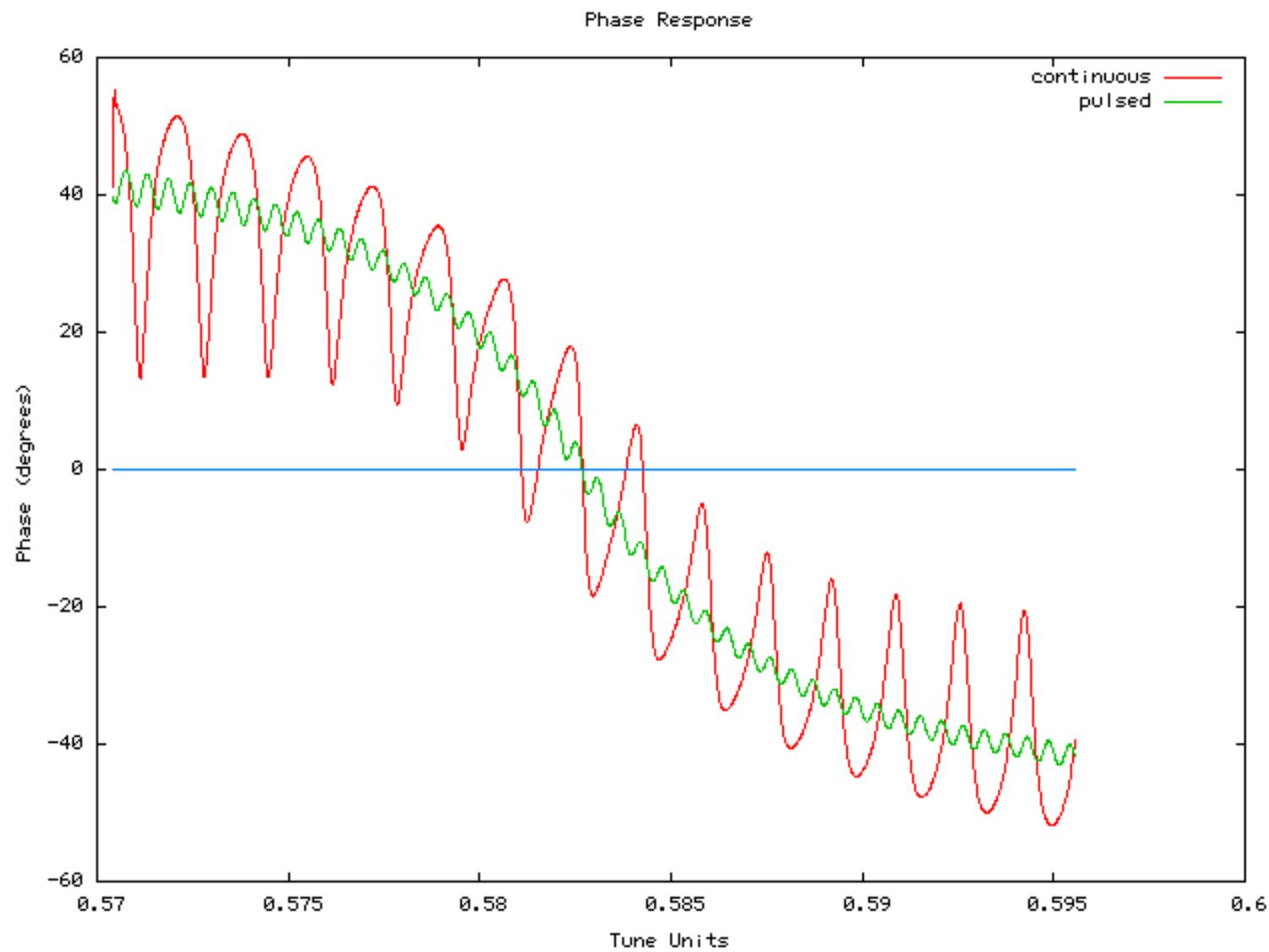
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How to Reduce Resolution BW

- In order to see the background tune and not the synchrotron lines, we must reduce the resolution BW.
 - ▶ Use a pulsed sine wave -- Use the "uncertainty principle" to our advantage. $FT(\text{pulse}) = \text{sinc}()$. BW of sinc given by size of main lobe = $2/(\text{pulse length})$.
 - ▶ For $t_{\text{on}} = 0.01 \text{ s} \Rightarrow 200 \text{ Hz}$ frequency spread. Compare this to synchrotron freq spacing of 84 Hz at 150 GeV .
 - ▶ $t_{\text{off}} = 0.03 \text{ s}$. Sufficient time for beam to damp

Open Loop Phase Response



Each Excitation has its advantages

■ Pulsed:

- ▶ Does not see synchrotron lines. Finds one background tune.
- ▶ Phase slope is gentle, therefore, there is slop.
- ▶ Possibility of overcoming coupling problem(?).

■ Continuous:

- ▶ Sees synchrotron lines, so will lock on arbitrary line.
- ▶ Phase slope is steep, so lock is precise.

Use Best of Both Worlds

- Use pulsed excitation p1 to obtain f_c .
- Use two continuous excitation p1s to sandwich f_c and obtain $f_{+/-}$.
- Use observation that $f_+ = f_c + n f_s$ and $f_- = f_c - m f_s$ with $m, n \in \mathbf{Z}$, to calculate a weighted f_c' .
- This is the reason why we are using 3 DDs

State of Hard Affairs

- Daughter card is complete.
 - ▶ No box yet (real soon now)
- RF modules not built yet. Should be pretty quick. Power splitters ordered should be here soon.
- Splitting signals from Schottkey detector and 21.4 MHz RF will be done when we have 3 day shutdown (soon).

State of Soft Affairs

- Altera
 - ▶ Bugs to SWAT.
- DSP
 - ▶ Bugs to SWAT.
- Rabbit microcontroller (ethernet)
 - ▶ Bugs to SWAT
- Control system software
 - ▶ Command line only (no GUI)
- There is NO synergy between all parts yet.

Conclusion

- **Hardware front:**

- ▶ DSP/daughtercard hardware complete.
- ▶ RF modules to be done.
- ▶ Splitting signals at A1 house for Schottkey signals and 21.4 MHz to be done.

- **Software front:**

- ▶ Software needs to be debugged and synergized.
- ▶ Bench characterization PLLs.
- ▶ First beam test probably end of March (still on schedule!)

- **Fake beam:**

- ▶ Jia Ning is working on a fake beam for PLL testing.